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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,732	07/22/2003	Kyoichi Suguro	04329.2344-02	6071

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EXAMINER	
LOKE, STEVEN HO YIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,732	SUGURO ET AL.	
	Examin r	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/609,107.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/22/03, 2/23/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

2. The abstract of the disclosure is objected to because the abstract should disclose the structure of the device instead of the method to make the device.

3. Figures 20A, 22 and 23 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The disclosure is objected to because of the following informalities: What is reference numeral 21 in fig. 4A? In page 56, line 26, it is unclear what is the limit of the delta. There is no 19B' (page 61, line 25) in fig. 19A. There is no line 19C-19C' (page 61, line 26) in fig. 19B. There are no reference numerals 75a and 75b (page 62, lines 6, 8) in the figures. There are no reference numerals 20 and 12 (page 66, lines 26-27) in the figures.

Appropriate correction is required.

6. Claims 1-3 are objected to because of the following informalities: Claim 1, line 1, the phrase "A semiconductor comprising:" is unclear whether it is being referred to "A

semiconductor device comprising:". Claim 1, line 10, claim 2, line 10, claim 3, line 10, the phrase "A MOS type element" is unclear whether it is being referred to "a MOS type element". Appropriate correction is required.

7. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of the semiconductor layer; and a MOS type element formed within a corresponding one of said element regions and having a gate insulating film and a metal gate electrode formed thereon, wherein: said gate insulating film and said metal gate electrode are formed on a top surface and sides of the semiconductor layer in said element region which are not covered with said element isolating insulating film as claimed in claim 3. The difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film as claimed in claim 4. The MOS element includes a source/drain region and the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region as claimed in claim 5.

8. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the structure of claims

3-5 as mentioned in paragraph 7 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Yamazaki.

In regards to claim 1, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103]; an element isolating insulating film [110] for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of said semiconductor layer; and a MOS type element formed within a corresponding one of the element regions and having a gate insulating film [118], wherein: a difference in height from the substrate between the top surface position of said element isolating insulating film and the top surface position of said semiconductor layer is at least three times as large as the thickness of said gate insulating film.

In regards to claim 2, Yamazaki shows all the elements of the claimed invention in fig. 8F. It is a semiconductor device, comprising: a substrate [101] having a semiconductor layer [103]; an element isolating insulating film [110] for partitioning said semiconductor layer into a plurality of element regions, the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of the semiconductor layer; and a MOS type element formed within a corresponding one of said element regions, wherein: a difference in height from the substrate between the top surface position of the semiconductor layer and the top surface position of the element isolating insulating film is at least 10 nm because the height is larger than the thickness of the gate insulating film [118] (col. 15, lines 10-14).

11. Claims 3 and 5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Ito (Applicants' IDS filed on 2/23/04).

In regards to claim 3, Ito shows all the elements of the claimed invention in figs. 1 and 2. It is a semiconductor device, comprising: a substrate [1] having a semiconductor layer [3]; an element isolating insulating film ([6a, 10] formed inside the trench) for partitioning said semiconductor layer into a plurality of element regions [3], the element isolating insulating film being formed on said substrate so as to penetrate said semiconductor layer and having a top surface projecting upward above a surface of the semiconductor layer [3]; and a MOS type element formed within a corresponding one of said element regions and having a gate insulating film [6] and a metal (tungsten silicide) gate electrode [7] formed thereon, wherein: said gate insulating film [6] and said metal

gate electrode are formed on a top surface and sides of the semiconductor layer in said element region (fig. 2) which are not covered with said element isolating insulating film.

In regards to claim 5, Ito further discloses the MOS element includes a source/drain region [8, 9] and the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is substantially at least a junction depth of said source/drain region.

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ito.

In regards to claim 4, Ito differs from the claimed invention by not showing the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film.

It would have been obvious to one having ordinary skill in the art at the time the invention was made for the difference in height from said substrate between the top surface position of said semiconductor layer and the top surface position of said element isolating insulating film is at least five times as large as a thickness of said gate insulating film because it depends on the desired isolation strength between the semiconductor elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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May 1, 2004

Steven Loke
Primary Examiner